

What is claimed is:

- 1    1.    A content addressable memory (CAM) device comprising:  
2            first and second rows of CAM cells;  
3            a first pair of match lines coupled to the first row of CAM cells;  
4            a second pair of match lines coupled to the second row of CAM cells; and  
5            a first logic circuit coupled to a first match line of the first pair of match lines and to  
6                    a first match line of the second pair of match lines, the first logic circuit being  
7                    configured to output a match signal in a first state if both the first match lines  
8                    indicate a match condition, and to output the match signal in a second state if  
9                    either of the first match lines indicates a mismatch condition.
- 1    2.    The CAM device of claim 1 further comprising:  
2            a first priority encoder coupled to the first match line of the first pair of match lines  
3                    and to the second match line of the second pair of match lines; and  
4            a second priority encoder coupled to the second match line of the first pair of match  
5                    lines and to the first match line of the second pair of match lines.
- 1    3.    The CAM device of claim 2 wherein the first priority encoder is also coupled to  
2            receive the match signal output from the first logic circuit.
- 1    4.    The CAM device of claim 1 further comprising a select circuit to output either a  
2            match signal present on the first match line of the first pair of match lines or the  
3            match signal output from the first logic circuit, depending on the state of a first  
4            select signal.
- 1    5.    The CAM device of claim 4 further comprising:

2 an interface to receive an instruction; and  
3 an control circuit coupled to receive the instruction from the interface and  
4 configured to output the first select signal in either a first logic state or a  
5 second logic state according to the instruction.

1 6. The CAM device of claim 5 wherein the control circuit is configured to generate the  
2 first select signal in a first state if the instruction indicates a single-word compare  
3 operation and in a second state if the compare instruction indicates a multiple-word  
4 comparand compare operation.

1 7. The CAM device of claim 4 further comprising a configuration circuit to store a  
2 mode value and configured to output the first select signal in either a first logic state  
3 or a second logic state according to the mode value.

1 8. The CAM device of claim 1 wherein each of the CAM cells within the first row of  
2 CAM cells comprises:  
3 a storage circuit; and  
4 first and second compare circuits coupled to the storage circuit.

1 9. The CAM device of claim 8 wherein the first match line of the first pair of match  
2 lines is coupled to the first compare circuit of each of the CAM cells within the first  
3 row of CAM cells, and wherein the second match line of the first pair of match  
4 lines is coupled to the second compare circuit of each of the CAM cells within the  
5 first row of CAM cells.

1 10. The CAM device of claim 1 further comprising a second logic circuit coupled to the  
2 second match line of the first pair of match lines and to the second match line of the

3 second pair of match lines, the second logic circuit being configured to output a  
4 match signal in the first state if both the second match lines indicate a match  
5 condition, and to output the match signal in the second state if either of the second  
6 match lines indicates a mismatch condition.

1 11. The CAM device of claim 10 further comprising a select circuit coupled to receive  
2 the match signal generated by the first logic circuit and the match signal generated  
3 by the second logic circuit, the select circuit being responsive to a select signal to  
4 output either the match signal generated by the first logic circuit or the match signal  
5 generated by the second logic circuit.

1 12. The CAM device of claim 11 further comprising a configuration circuit to store a  
2 mode value and to output the select signal in either a first logic state or a second  
3 logic state according to the mode value.

1 13. The CAM device of claim 11 further comprising:  
2 an interface to receive a compare instruction; and  
3 a control circuit coupled to receive the instruction from the interface and configured  
4 to output the select signal in either a first logic state or a second logic state  
5 according to the compare instruction.

1 14. The CAM device of claim 1 further comprising a storage circuit coupled to the first  
2 match line of the first pair of match lines to store a match value indicative of the  
3 state of the first match line of the first pair of match lines.

1 15. The CAM device of claim 14 further comprising a logic AND gate coupled to  
2 receive the match value from the storage circuit and coupled to the first match line

3 of the second pair of match lines.

1 16. The CAM device of claim 1 wherein the first logic circuit comprises an AND gate  
2 having a first input coupled to the first match line of the first pair of match lines and  
3 a second input coupled to the first match line of the second pair of match lines.

1 17. The CAM device of claim 16 further comprising storage circuits coupled to the first  
2 match lines to store the states of respective match signals thereon and to output the  
3 stored states of the respective match signals to the first and second inputs of the  
4 AND gate.

1 18. The CAM device of claim 1 further comprising:  
2 a first pair of precharge circuits coupled respectively to the first match lines of the  
3 first and second pairs of match lines; and  
4 a second pair of precharge circuits coupled respectively to the second match lines of  
5 the first and second pairs of match lines.

1 19. The CAM device of claim 18 further comprising circuitry to assert a first precharge  
2 enable signal to enable the first pair of precharge circuits to precharge the first  
3 match lines during a first interval, and to assert a second precharge enable signal to  
4 enable the second pair of precharge circuits to precharge the second match lines  
5 during a second interval.

1 20. The CAM device of claim 19 wherein the CAM device further comprises control  
2 circuitry to initiate a first compare operation in the first and second rows of CAM  
3 cells during the first interval and to initiate a second compare operation in the first  
4 and second rows of CAM cells during the second interval, the first compare

5 operation producing match results on the second pair of match lines and the second  
6 compare operation producing match results on the first pair of match lines.

1 21. A content addressable memory (CAM) device comprising:  
2 a plurality of row pairs of CAM cells, wherein each row of CAM cells in a row pair  
3 is coupled to a plurality of match lines; and  
4 a plurality of logic circuits each having inputs coupled to the plurality of match  
5 lines of a corresponding row pair of CAM cells, each of the plurality of logic  
6 circuits configured to selectively combine match results on the plurality of  
7 match lines of both rows of a corresponding row pair and output a composite  
8 match signal.

1 22. The CAM device of claim 21 wherein each CAM cell within each row of CAM  
2 cells in a row pair includes a plurality of compare circuits coupled respectively to  
3 the plurality of match lines.

1 23. The CAM device of claim 22 wherein each CAM cell within each row of CAM  
2 cells in a row pair includes a memory cell coupled to each of the plurality of  
3 compare circuits within the CAM cell.

1 24. The CAM device of claim 21 wherein each of the plurality of logic circuits  
2 comprises a logic AND gate to logically AND the match results on a respective pair  
3 of match lines of the plurality of match lines.

1 25. A content addressable memory (CAM) device comprising:  
2 a plurality of CAM cells each including a first compare circuit and a second  
3 compare circuit;

4 a plurality of first match lines coupled to the first compare circuits included in the  
5 plurality of CAM cells;  
6 a plurality of second match lines coupled to the second compare circuits included in  
7 the plurality of CAM cells; and  
8 a plurality of logic circuits each coupled to a respective one of the first match lines  
9 and a respective one of the second match lines, each logic circuit being  
10 configured to output a match signal having a state according to the state of the  
11 one of the first match lines and the state of the one of the second match lines.

1 26. The CAM device of claim 25 wherein each of the plurality of logic circuits is  
2 configured to output a match signal in a first state if the one of the first match lines  
3 indicates a match and the one of the second match lines indicates a match, each of  
4 the plurality of logic circuits being further configured to output a match signal  
5 having a second state if either of the one of the first match lines and the one of the  
6 second match lines indicates a mismatch.

1 27. The CAM device of claim 26 wherein each of the plurality of logic circuits  
2 comprises a logic AND gate having a first input coupled to the one of the first  
3 match lines and a second input coupled to the one of the second match lines.

1 28. The CAM device of claim 27 wherein each of the plurality of logic circuits further  
2 comprises a select circuit having a first input coupled to an output of the logic AND  
3 gate and a second input coupled to the one of the first match lines.

1 29. The CAM device of claim 28 wherein the select circuit is a multiplexer.

1 30. The CAM device of claim 25 further comprising a priority encoder coupled to

2 receive the match signals output by the plurality of logic circuits.

1 31. A method of operation within a content addressable memory (CAM) device, the  
2 method comprising:  
3 simultaneously performing first and second compare operations in an array of CAM  
4 cells to generate first and second sets of match signals; and  
5 logically combining the first set of match signals with the second set of match  
6 signals to generate a set of resultant match signals.

1 32. The method of claim 31 wherein simultaneously performing first and second  
2 compare operations in an array of CAM cells comprises simultaneously providing  
3 first and second comparands to the array of CAM cells via first and second compare  
4 ports, respectively.

1 33. The method of claim 32 wherein the CAM cells in the array of CAM cells are  
2 arranged in rows, each row of CAM cells being coupled to a corresponding pair of  
3 match lines, and wherein simultaneously performing first and second compare  
4 operations in the array of CAM cells further comprises receiving the first and  
5 second comparands in each of the rows of CAM cells, each row of CAM cells  
6 outputting a first match signal on a first match line of the corresponding pair of  
7 match lines according to whether the first comparand matches a value stored within  
8 the row of CAM cells, and each row of CAM cells outputting a second match signal  
9 on a second match line of the corresponding pair of match lines according to  
10 whether the second comparand matches the value stored within the row of CAM  
11 cells.

1 34. The method of claim 31 wherein simultaneously performing first and second  
2 compare operations comprises simultaneously comparing a value stored within each  
3 CAM cell of the CAM array with a portion of a first comparand value and a portion  
4 of a second comparand value.

1 35. The method of claim 31 wherein logically combining the first set of match signals  
2 with the second set of match signals comprises combining each match signal of the  
3 first set of match signals with a respective match signal of the second set of match  
4 signals to generate a respective one of the resultant match signals.

1 36. The method of claim 35 wherein combining each match signal of the first set of  
2 match signals with a respective match signal of the second set of match signals  
3 comprises logically ANDing each match signal of the first set of match signals with  
4 the respective match signal of the second set of match signals to generate the  
5 respective one of the resultant match signals.

1 37. The method of claim 31 further comprising selecting either the set of resultant  
2 match signals or the first set of match signals to be output as a selected set of match  
3 signals.

1 38. The method of claim 37 further comprising generating a match address based on the  
2 selected set of match signals.

1 39. A content addressable memory (CAM) device comprising:  
2 an array of CAM cells;  
3 means for simultaneously performing first and second compare operations in the

4           array of CAM cells to generate first and second sets of match signals; and  
5           means for logically combining the first set of match signals with the second set of  
6           match signals to generate a set of resultant match signals.

1   40.   The CAM device of claim 39 wherein the means for simultaneously performing  
2           first and second compare operations in the array of CAM cells comprises means for  
3           simultaneously providing first and second comparands to the array of CAM cells  
4           via first and second compare ports, respectively.

1   41.   The CAM device of claim 39 wherein the means for simultaneously performing  
2           first and second compare operations comprises means for simultaneously  
3           comparing a value stored within each CAM cell of the CAM array with a portion of  
4           a first comparand value and a portion of a second comparand value.

1   42.   The CAM device of claim 39 wherein the means for logically combining the first  
2           set of match signals with the second set of match signals comprises means for  
3           combining each match signal of the first set of match signals with a respective  
4           match signal of the second set of match signals to generate a respective one of the  
5           resultant match signals.

1   43.   The CAM device of claim 39 further comprising means for selecting either the set  
2           of resultant match signals or the first set of match signals to be output as a selected  
3           set of match signals.

1   44.   The CAM device of claim 43 further comprising means for generating a match  
2           address based on the selected set of match signals.